# EUVL HVM Insertion Timing and Scaling

**Panel Discussion**
**2012 International Workshop on EUV Lithography**
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# The Panelists

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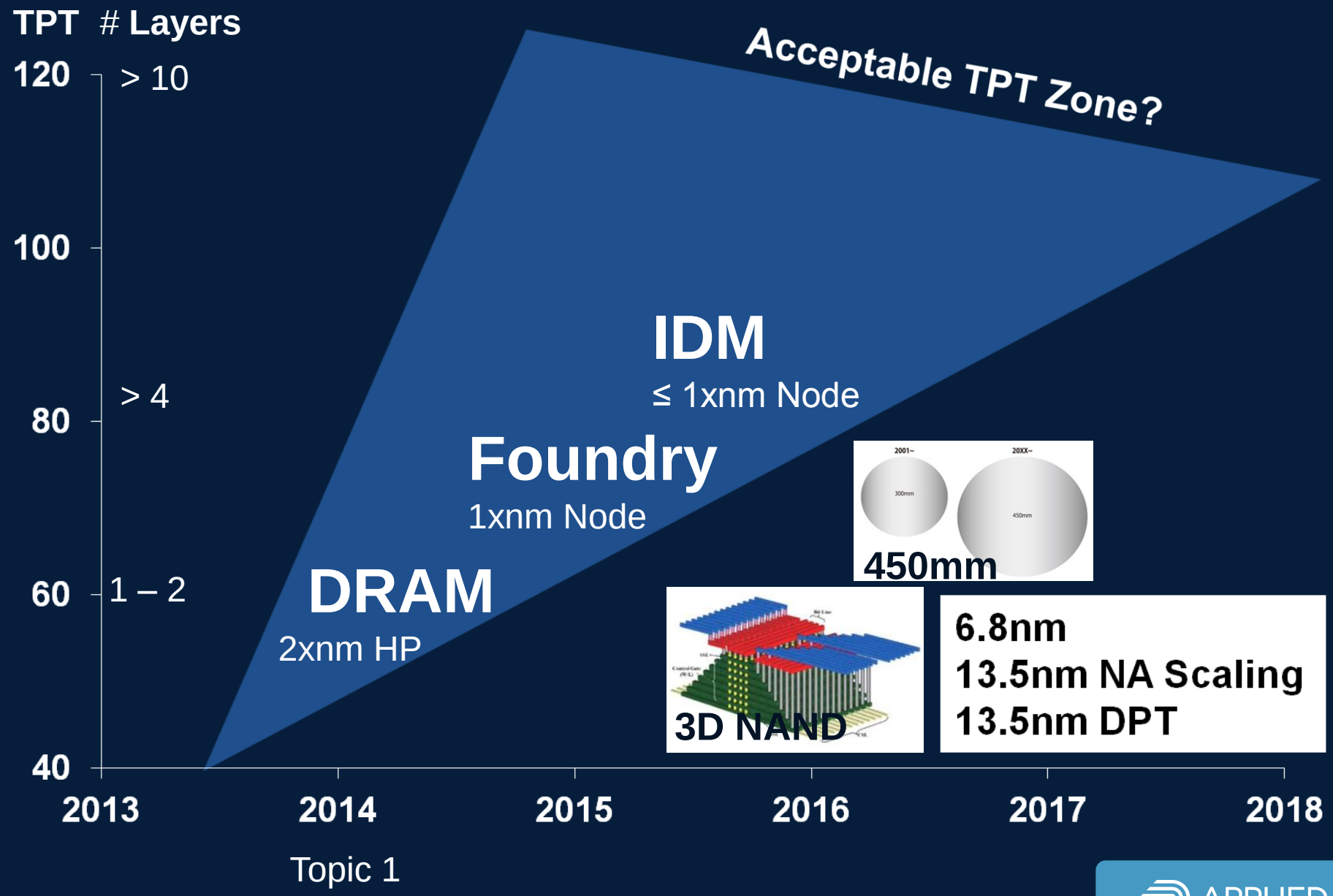
# EUV HVM by Device = f (TPT, Die-Size, Scaling Path, COO)




Topic 1



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# Topic 1
## Timing of EUV HVM Insertion for the Industry?

## Minimum Throughput Needs?

## By Device
- NAND
- DRAM
- IDM
- Foundry

## By Function
- Line/Space
- CON/Via

# EUV Ecosystem Requirements:- Changes relative to 193nm infrastructure and critical issues to resolve.

| EUV Infrastructure | Current | Requirements | Challenges |
|---|---|---|---|
| Source IF, Watts/Uptime | ~30W | 100-200 Watts/85% | Timing |
| Mask Defects<br>Inspection/Metrology | 10 @ 60nm | 0.01@20nm<br>0 Die Yield Loss | “Printability”<br>Fab & Maskshop |
| Mask HVM Lifetime | | 0 printable defects &<br>Reflectivity Change<br>Per x Runs. | Effective Cleans<br>Reflectivity,<br>Flatness |
| Resist Resolution<br>LWR<br>Dose to Size | 16nm<br>3σ=3nm<br>33mJ/cm2 | <16nm<br>3σ<1nm (≤1xnm Node)<br>10mJ/cm2 at Min.CD. | |
| Pattern Collapse | | 0 Integrated Defects<br>>10% EL at 200nm<br>DOF | Plasma Cleans,<br>Highly Selective<br>Films/Etches,<br>Interface Control |

Acknowledgements:Sematech/Intel/Global-Foundries

Topic 2

# Topic 2

## EUV Ecosystem Requirements?

- Changes relative to 193nm infrastructure and critical issues  to resolve.

## Minimum Requirements?

- Source Power
- OPC needs
- Mask Requirements (Defects, cleans and Metrology)
- Resist Issues

# EUVL 5-7nm ITRS Node Scaling Paths (2017-2020)

| EUV Scaling Paths | Issues/Challenges (450mm?) |
|---|---|
| **8-12nm HP Patterning Paths with EUVL for 2017-2020** | |
| **13.5nm Double Patterning, Lower K1** | **193nm Like RET (ePSM,aPSM?),COO** |
| **13.5nm >0.5 "Hyper NA"** | **Power Loss** |
| **6.8nm Beyond EUV (Soft X-rays)** | **Time, New Infrastructure** |

| | Source | Mirrors | Peak R% |
|---|---|---|---|
| **13.5nm** | **Sn** | Mo/Si/B4C | >70% |
| **6.Xnm** | **Tb/Gad** | LaN/B4C | Empirical? |
| **4x Multi-Layer Stacks Needed at 6.xnm, Much Smaller Spectral band-Width, Increased Interface Complexity** | | | |

Topic 3

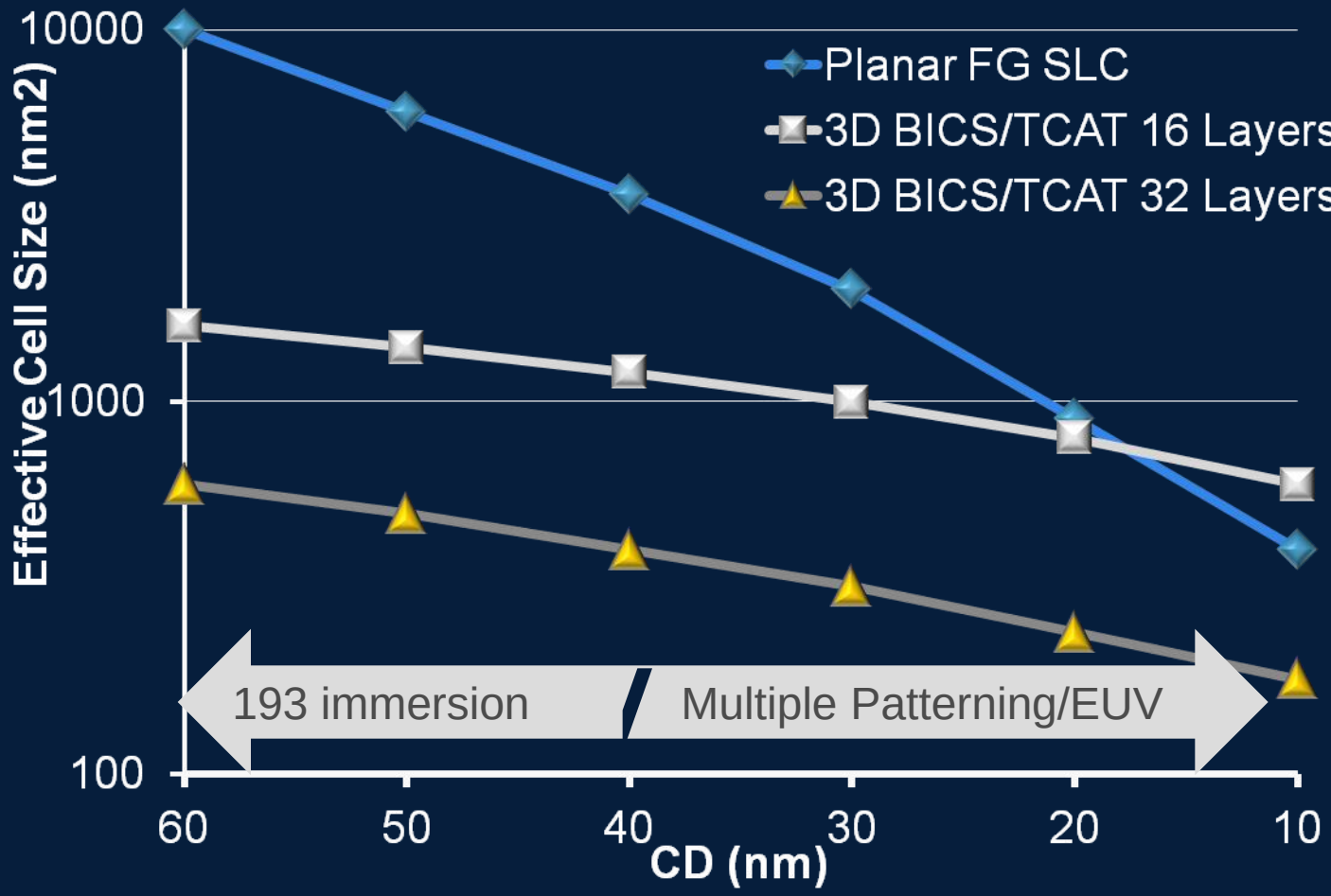
# Topic 3

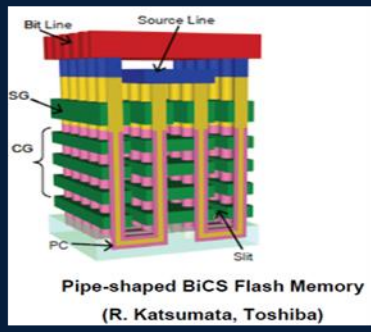
EUVL scaling paths to meet the ITRS timelines for 5-7nm nodes (2017-2020)?

- Lower K1/Double Patterning
- NA scaling to NA>0.5
- 6.8nm Soft X-ray Lithography
  New infrastructure (optics, resists, power requirements again)

# BackUp

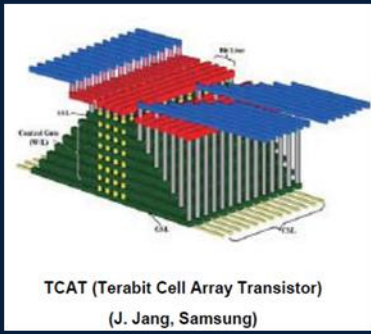
# 1X Planar NAND Scaling Slowing
# 3D NAND Development Ramps Up …



Pipe-shaped BiCS Flash Memory
(R. Katsumata, Toshiba)

- Planar NAND Ends Around 13-15nm
- 3D Memory Stays at >40nm Lithography and Scales Vertically


TCAT (Terabit Cell Array Transistor)
(J. Jang, Samsung)

## 3D NAND Scales Vertically, Bypasses Litho Scaling

**Acknowledgements:- International Memory Workshops**



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